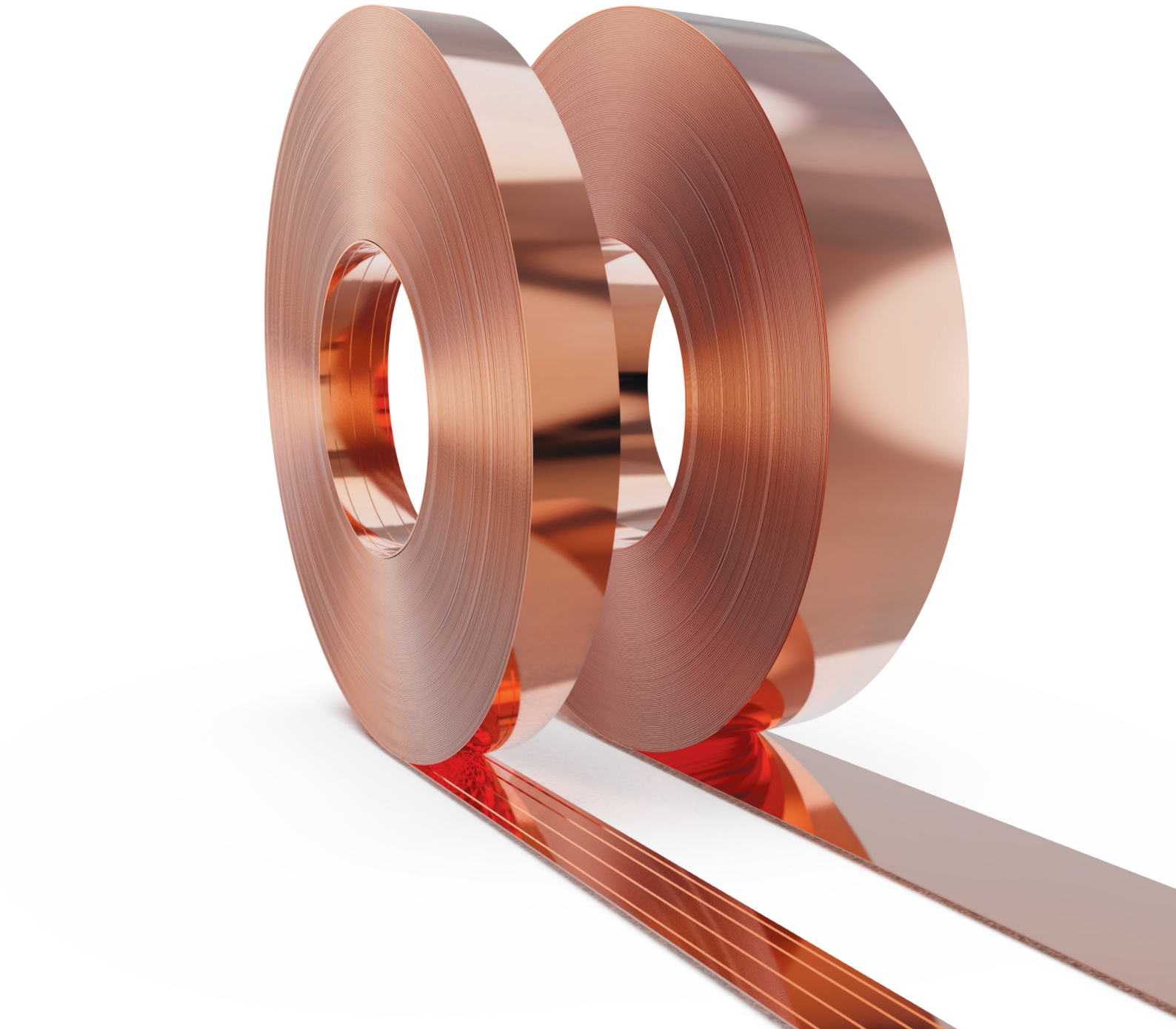
wieland

Strip for semiconductor packages



Strip for semiconductor packages

Requirements for leadframe strip used for IC's & discrete packages

Strips for IC leadframes and discrete semiconductor packages call today for specially tailored copper alloys requiring the following properties:

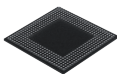
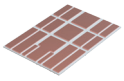
- special leadframe surface qualities to meet plating and wire bonding requirements
- material properties adjusted to today's semiconductor packaging assembly processes
- high strength copper alloys allowing to produce matrix leadframes in large width
- softening resistant alloys suitable for high die bonding temperatures
- alloy and temper properties allowing to etch strips with high productivity
- tight dimensional tolerances
- low internal tension allowing to stamp or etch high pin semiconductor frames with excellent lead co-planarity

Requirements for copper strip used for Power & Heat-spreader

- copper with very high electrical and thermal conductivity
- good surface properties to allow perfect plating and marking
- good stamping and forming properties
- chemical composition of copper alloys to meet RoHS requirements

Typical applications

The following table provides an overview of the usage of Wieland alloys within the semiconductor packaging industry.

Appli-cation	Heatspreader	Integrated circuit (IC)				Discrete				Power Electronics
Package	BGA/LGA/PGA 	QFN/DFN/SON 	QFP 	TSOP 	DIP 	SOT 	TO220/TO247 	LED 	DPAK 	DCB 
K09	•									•
K32	•									
K55		•	•	•						
K65		•	•	•	•	•		•		
K75						•		•		
K80							•	•	•	

Material properties

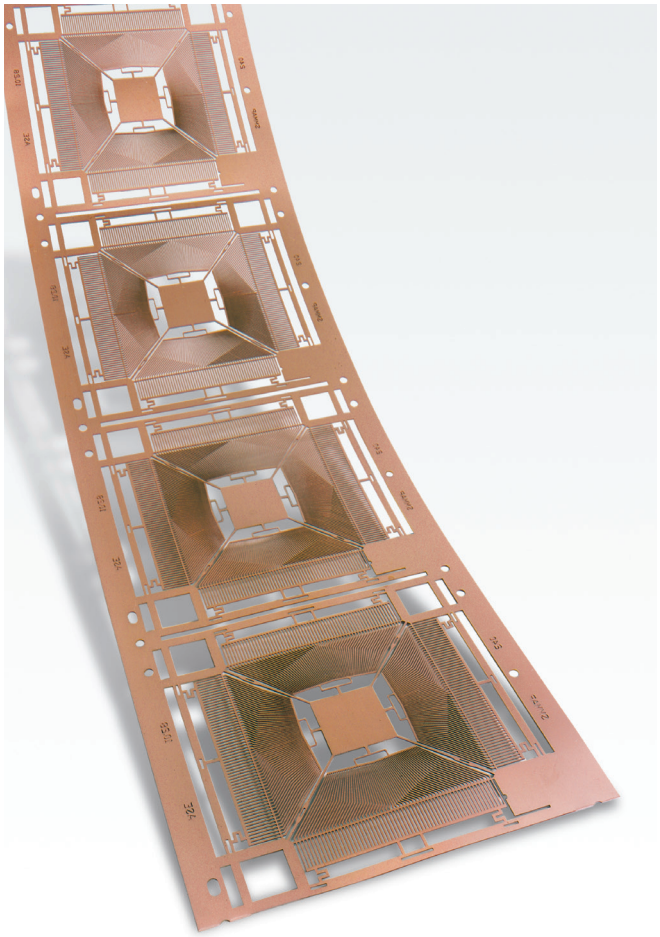
Wieland materials for semiconductor packages comply with established international standards such as EN, ASTM and JIS. The following table provides an overview of the mechanical and physical properties of Wieland alloys used in semiconductor packaging. For further details kindly refer to the specific datasheet.

Alloy	UNS	Chemical composition (nominal) wt [%]	Electrical conductivity [%] IACS	Thermal Conductivity [W/(mK)]*	Common Temper **	Tensile strength [Mpa]	Yield strength [Mpa]	Elongation A50 [%]	Hardness HV *
K09	C10100	Cu ≥ 99.99	100	391	R240	240-300	≥180	≥8	65-95
K32	C11000	Cu ≥ 99.90	100	390	R240	240-300	≥180	≥8	65-95
K55	C70250	Ni 3 Si 0.65 Mg 0.15 Cu balance	43	190	TR02 Half Hard	608-725	550-650	≥6	180-220
					R800 Spring Hard	800-900	≥750	≥1	230-270
K65	C19400	Fe 2.4 Zn 0.12 P 0.03 Cu balance	64	260	R370 Half Hard	370-430	≥330	≥6	120-140
					R420 Full Hard	420-480	≥380	≥3	130-150
					R470 Spring Hard	470-530	≥440	≥4	140-160
					R530 Extra Spring Hard	530-570	≥470	≥5	150-170
K75	C18070	Cr 0.3 Ti 0.1 Si 0.02 Cu balance	83	310	TR02	430-570	≥370	≥7	130-150
					R460 Full Hard	460-560	≥400	≥9	140-170
K80	C19210	Fe 0.1 P 0.03 Cu balance	91	350	R360	360-440	≥260	≥3	100-130

**: for reference only*

***: typical temper shown; for more details see alloy data sheets*

Strip for leadframe based packages



Leadframes

Leadframes for IC or discrete semiconductors are either stamped or etched. Each process requires different strip properties. As such, Wieland delivers optimized strip qualities for stamped and etched leadframes.

While stamping qualities are typically delivered in a slightly oiled condition to enhance the stamping process, etched strips typically require dry surfaces. Both qualities require base materials with an optimized stress distribution in order to allow stamping and etching of high pin count leadframes with convincing results.

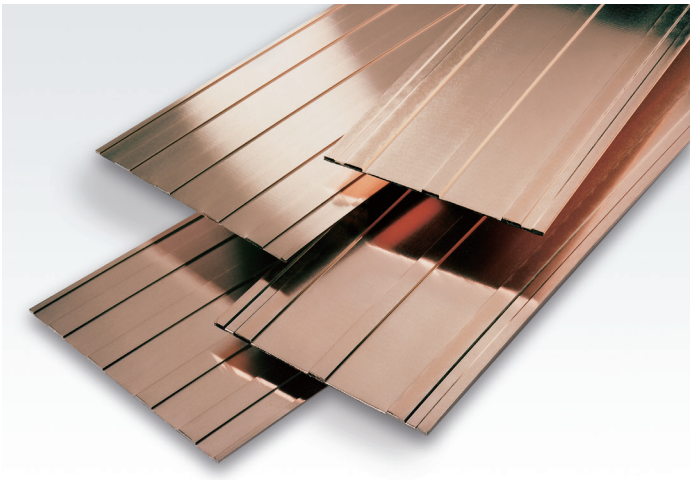
Many semiconductor packages like QFN/DFN/SON require in their production, half etching processes, meaning that the strip thickness is reduced by the etching medium. In order to achieve a proper solution even for such requirements special qualities have been developed to guarantee best half etching results. These qualities are limited to certain alloy/thickness combinations.

Resistance to softening

Many of today's discrete leadframes require a die bonding attachment process at temperatures exceeding 400 °C. In addition, high pin IC leadframes are often annealed after stamping at temperatures exceeding 450°C requiring special softening resistant alloys and tempers. For these applications Wieland developed special softening resistant alloys with convincing irreversible lengthening properties.

Contour-milled strip

Contour milling is a process to produce dual-gauge and multi-gauge strip. This type of strip opens up new possibilities of producing components with sections of different thicknesses. Coining in the stamping tool is no longer necessary.



Strip for power electronics

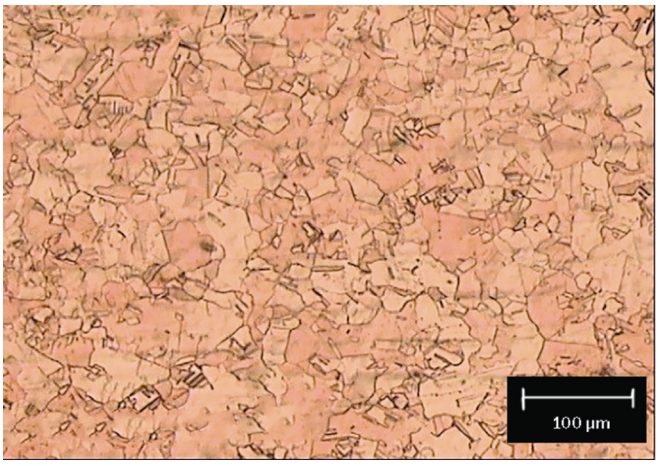
DCB copper strip

DCB spoken in words means "Direct Copper Bonding" and is a technology of bonding pure copper strip to the surface of a ceramic substrate by a high temperature process. The ceramic substrate will be covered on both sides by the pure copper strip. The top copper layer will become segmented into different areas, on which the power electronic chips as well as the bond wires are bonded to. The bottom layer stays plain and unsegmented. It will be attached to a heat sink of the power electronic module.

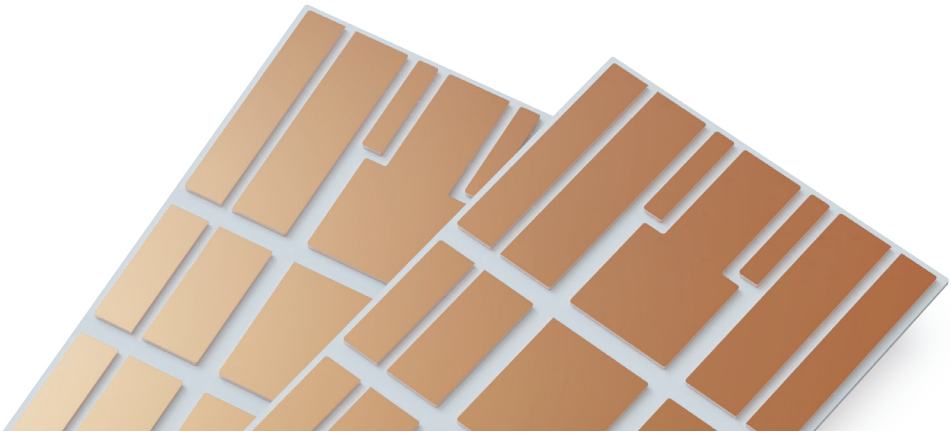
Due to the high temperature during the DCB process, there is a special requirement to the pure copper strip: Grain growth must be restricted and average grain size after temperature treatment must be below a value of around 100 µm. This is only fulfilled by a certain grade, called "DCB copper strip".

DCB copper strip	
Material designations	OFE-Cu, C10100, Wieland-K09
Electrical conductivity	100% IACS
Tensile strength	330-390 MPa
Special properies	Grain growth restriction during heat treatment
Available thicknesses	0.20, 0.25, 0.30, 0.40, 0.50, 0.60mm

DCB-requirements **not fullfilled**.



DCB-requirements **fullfilled.**



Properties of leadframe strip

Strip surface qualities

Strip for semiconductor packages requires surfaces without imperfections such as scratches, pits, dents, rolling marks and defects that may cause functional problems on the final application. Different alloys and thicknesses however lead to different surface appearances.

In order to meet the stringent surface requirements for bondable semiconductor packages, Wieland has developed several strip surface qualities providing a unique solution for each leadframe application.

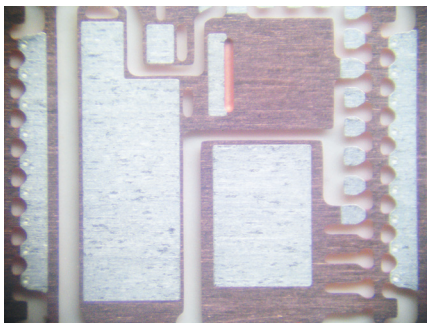
	Power Strip Quality (Power Quality)	Leadframe Quality Brushed	Leadframe Quality	Leadframe Quality Extra
Rmax	Max. 3.0 (max 1.8*)	Max. 1.0	Max. 1.0	Max. 1.0 (max. 0.8*)
R_a	Max. 0.16	Max. 0.13	Max. 0.13	Max. 0.13
Alloy	K09, K32, K80	K65, K75, K80	K55, K65	K55, K65
Specifics	Standard surface quality for power	Standard surface quality for smart power	Standard surface quality for IC	Further improvement surface quality compared to LFQ
Application (example)	Power	Smart Power Discrete, IC	IC (stamped parts)	IC (high end etched parts and stamped parts)

**: achievable with additional effort*

High speed plating (HSP) surface quality

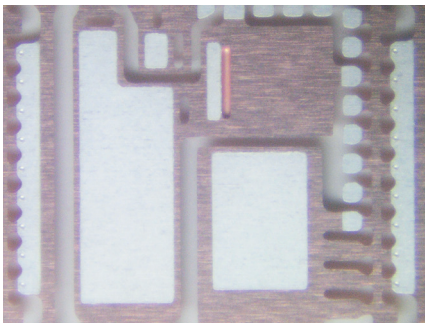
HSP is a solution for homogeneous plating with no surface micro-etching at customer process prior plating. It is mainly available for K65 (C19400) FH 0.203mm and ESH 0.152mm (other tempers and thicknesses can be inquired).

The plating type is suitable for Silver (Ag) or Nickel (Ni). Common packages include: QFN, QFP, SOIC etc. Other potential applications are LED with Hi-GAM or Ag-plated surface for 3D laser marking.



Standard strip surface plated with Ag:

patchy and in-homogeneous



HSP quality strip surface plated with Ag:

throughout homogeneous

Tolerances

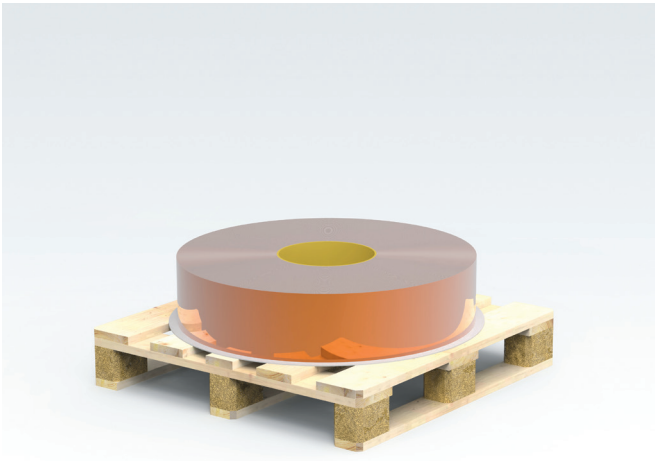
Wieland's customers process strip for semiconductor packages with high-precision equipment. This results in particularly high requirements for the tolerances and the geometric properties of the strip. Thickness and width tolerances can be restricted to the tightest of margins compared to the relevant standards. Special measures can be taken during strip production in order to minimize geometric deviations such as camber, coil set and cross bow.

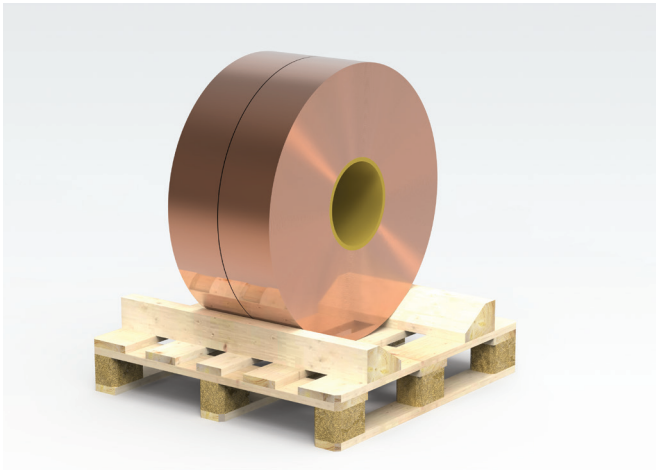
strip thickness (mm)	thickness tolerance (mm)	width tolerance (mm)	Tolerances valid for a maximum width of
<0.30	+0.005	+0.050	200mm*
>0.30-0.50	+0.007	+0.070	200mm*
>0.50–0.80	+0.010	+0.080	200mm*
>0.80–1.50	+0.013	+0.100	135mm*
>1.50–2.00	+0.015	+0.150	135mm*

**: Tolerances for wider width to be agreed upon on basis of individual feasibility studies.*

Delivery formats

Due to the very high surface requirements for semiconductor strips, the material is delivered only in coil form. Furthermore, coils are the simplest and therefore the most economical delivery format strip. They are packed horizontally or vertically on square or round pallets, the size of which is matched to the outer diameter of the coils. In order to support high productivity for our customers, we deliver as well big coils with outer diameter of up to 1,450 mm providing several kilometers of strip length.





	Inner diameter (mm)	Outer diameter (mm)
K09	400	Max 1450
K32	400	Max 1450
K55	400	Max 1300
K65	400	Max 1300
K75	400	Max 1300
K80	400	Max 1450

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02/2022 RP.TMA.UL/Zr 0,0 (MC.ED.UL/Ru)